Dr. Ryan Keech is an Assistant Leader in the Advanced Materials and Microsystems Group at MIT Lincoln Laboratory with expertise in microfabrication and process integration for CMOS technologies. His research efforts involve developing novel process and integration solutions to further the utility, reliability, and performance of transistors and advanced devices in extreme environments.

Prior to joining Lincoln Laboratory, Keech worked as a pathfinding engineer in Intel Corporation's Logic Technology Development group, where he focused on novel epitaxial source/drain solutions for the 7 nm, 4 nm, and 20 Å technology nodes and for beyond-silicon devices. Named an "Intel Innovator" from 2018 to 2020, Keech has 14 patents issued or pending from this work, which has been recognized in several Intel divisional awards.

Keech holds a BS degree in materials science and engineering from the University of Connecticut and a PhD degree in the same field from the Pennsylvania State University, where he studied as a 3M Fellow. His doctoral work focused on characterizing the changes in ferroelectric and piezoelectric responses of thin films upon dimensional scaling and developing microfabrication methods to yield enhanced functional properties. His work was leveraged in the fabrication of the novel piezoelectronic field effect transistor in a collaboration with IBM.